SD Association

# SD Express Memory Cards with PCIe® and NVMe™ Interfaces

**Following specifications are covered:**

- **SD7.0: SD Express card with PCIe 3.1 interface**
- **SD7.1: microSD Express card with PCIe 3.1 interface**
- **SD8.0: SD Express with dual lane and PCIe 4.0**

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# Executive Summary

In March 2020, the SD Association (SDA) released its SD 8.0 specification (SD8.0) offering the fastest SD Express card capable of delivering gigabyte speeds via dual PCIe® lane support and PCIe 4.0 with NVMe™. This update follows two earlier SD Express specifications:

- SD 7.1 specification (SD7.1) introduced the microSD Express card in February 2019. microSD Express incorporates the SD Express interface, comprised of the PCIe 3.1 and NVMe interface with the legacy SD interface, into the microSD form factor.

- SD 7.0 specification (SD7.0) introduced two major new functions in June 2018:
  - SD Express: Added the PCIe 3.1 and NVMe interface, to full-sized SD memory cards alongside legacy SD interface.
  - SD Ultra Capacity (SDUC): Expanded the potential maximum SD memory card capacity from 2TB to up to 128TB.

Hereafter, the term SD Express in this document refers to both form factors – full size SD and microSD, unless otherwise specified.

PCIe and NVMe are known worldwide for their high bandwidth and low latency storage capabilities. In anticipation of the next generation of high performance mobile computing requirements, adding both of these architectures delivers faster access to data files than the various legacy SD platforms achieving speeds of up to ~1GB/s (985 MB/s) with PCIe 3.1 x1 (single lane) and up to ~4GB/s (3938MB/s), with PCIe 4.0 x2 (dual lane), supporting content applications and data generated by highly demanding system architectures. This new protocol allows SD Express memory cards to serve as removable ***Solid State Drives (SSD)***.

The speeds delivered by SD Express are essential for high-resolution content applications such as: super-slow motion video, RAW continuous burst mode photography, 8K video capture and playback, 360 degree video, speed hungry applications running on cards and mobile computing devices, ever-evolving gaming systems, multi-channel Internet-Of-Things (IoT) devices, numerous automotive storage needs, to name a few. microSD Express opens expanded opportunities for SD in mobile devices, gaming, drones, IoT and other applications that require high performance removable memory cards.

# The Insatiable Need for More Capacity, Performance and Modern Protocols

In SD7.0, the SDA extended the limits of traditional SD memory cards' capacity to meet the ever growing needs of users everywhere. The new SDUC surpasses SDXC's 2TB maximum, allowing micro or full size SD memory cards to store up to 128TB, regardless of interface type: UHS-I, UHS-II, UHS-III or SD Express. However, the SD Express card with its PCIe and NVMe interfaces is the revolutionary addition to SD7.0.

With SD8.0, the main addition is the upgrade of the PCIe interface to PCIe 4.0 with up to ~2GB/s and the option to have two PCIe lanes supported, either PCIe 3.1 x2 (up to ~2GB/s) or PCIe 4.0 x2 (up to ~4GB/s). These new capabilities are limited to the full size SD card for now.

A few major market conditions have raised the requirements for removable memory cards with higher speeds, improved protocols and faster interfaces:

**Applications Demand Capacity**

- Demand for higher capacity memory grows continuously with the advancement of applications such as higher resolution videos, 3D graphic games, social media, drones, action cameras, 360° cameras, virtual reality, and streaming video content that is stored on SD memory cards for offline usage.
- Higher capacity cards require ever-faster speeds to move content quickly.

**Evolving Mobile Computing Infrastructure**

- Growing performance levels of input/output (IO) communication interfaces with either wireless such as Wi-Fi/Wi-Gig, or wired such as USB 3.
- Rapid developments in application processor technology, including multi cores, speed, RAM increases, etc.
- Embedded storage is transitioning to more advanced protocols opening new opportunities, including UFS, PCIe and NVMe.
- These evolving technology trends push removable memory interfaces requirement for additional higher random and sequential performance requirements.

**Client Computing, Imaging and Automotive**

- Client computing is moving rapidly from SATA to PCIe Gen3, multi-channel and Gen4.
- Various memory related emerging markets require high-speed memory interfaces and multi-channel operations. A sample of markets include autonomous vehicles and connected cars with multi sensor data collection and processing, multi-channel video capture for IoT devices.
- The imaging market that is already trending toward UHS-II/III or PCIe is showing growing demand for high speed due to 8K video capture, RAW high resolution videos and bursts, and 360 degree high resolution videos.

These evolving technology trends signal a demand for memory cards with high performance sequential and random access provided by SD Express.

The major operating systems now allow applications to start-up directly from an SD memory card. SD memory cards may now be used in Google Android devices as embedded memory or extended system storage for video/audio content as well as for storing and running apps. Running Android applications from a card requires higher random performance and sequential performance capabilities.

In 2016 and 2017, SDA introduced the Application Performance Classes A1 and A2 to ensure a certain level of random performance of SD memory cards under given conditions. While the sequential and random performance of the existing SD interface may be good enough for most of today's uses of cards, new applications will undoubtedly require ever-higher performance levels that can be achieved with SD Express using its added higher performance PCIe and NVMe interfaces.

# SD Express with PCIe and NVMe Benefits Everyone

SD Express includes a UHS-I interface with the PCIe and NVMe interfaces. The general idea is utilization of the existing well-known and familiar protocols defined by PCI SIG and NVMe Forum. By relying on successful protocols already in the marketplace, the SDA gives the industry an advantage by leveraging existing test equipment and saving in development processes. When companies use existing building blocks and existing designs, this translates to cost savings and an improved bottom line.

With existing support of major operating systems and popularity of drivers supporting PCIe and NVMe, the market adoption of SD Express should be easy.

Figure 1 shows the strength of SD Express by combining PCIe and NVMe with SD:

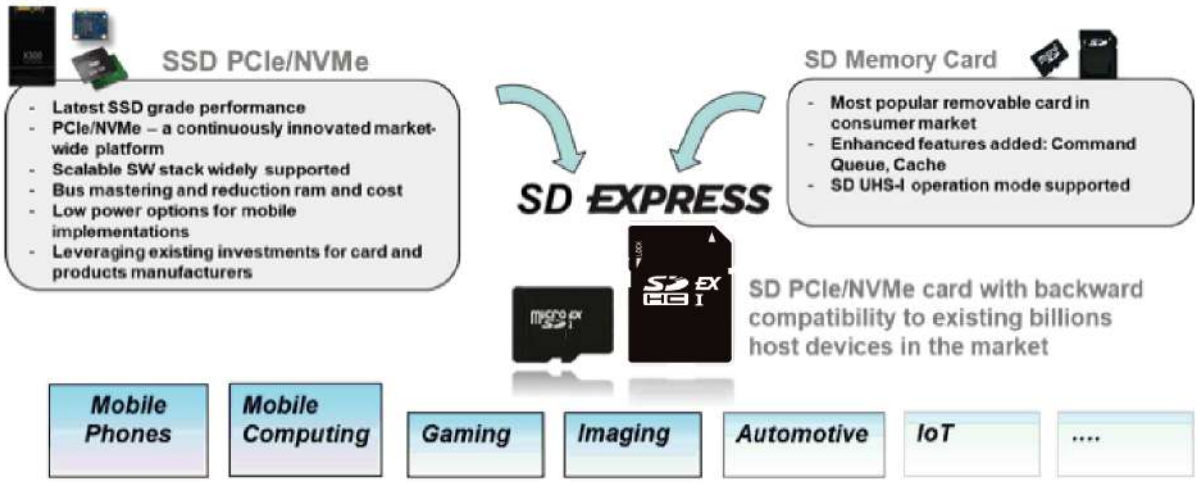


*Figure 1 SD Express – The best of all worlds*

# Understanding SD Express

SD Express was introduced in full size SD and microSD form factors is as follows:

- A microSD Express card shown in Figure 2 includes a second row of pins found on microSD UHS-II cards; however, the pins of the second row were shortened and moved upward in SD7.1. This form factor may support a single lane PCIe Gen 3 (as defined in SD7.1).
- The full size SD Express card described in Figure 3 uses the same pins and connectors as defined for existing SD UHS-II in SD7.0. This form factor may support a single lane PCIe Gen 3 (as defined in SD7.0) or PCIe Gen 4 (as defined in SD8.0).

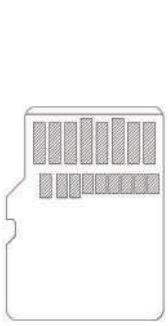

*Figure 2 –microSD Express pin layout*

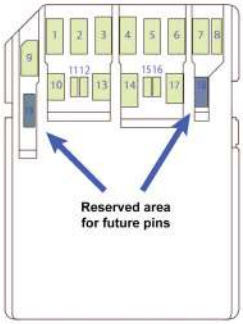


*Figure 3 – Full size SD Express pin layout*

*Figure 4 – Full size SD Express with two PCIe lanes pin layout*

- The full size SD Express shown in Figure 4 adds a third row of pins to support two PCIe lanes of either PCIe Gen3 x2 or PCIe Gen4 x2, as defined in SD8.0.
- All form factors feature new PCIe and NVMe interfaces. The differential interface of SD Express card with single lane PCIe uses the same pads as of the SD UHS-II differential interface pads found in the second row of pins. The PCIe's REFCLK along with the side band signals CLKREQ# and PERRST# are shared with the existing SD UHS-I, leveraging the first row of pins.
- The first row of pins is also the SD UHS-I interface, delivering full backward compatibility and interoperability with billions of existing SD host devices.
- SD Express cards cannot support UHS-II interface.
- SD7.0 and SD7.1 define full size SD and microSD form factors using two power supplies, a traditional 3.3 volt and 1.8 volt. An optional 1.2v supply is planned for future form factors requiring additional pins (#18 for full size and #17 for microSD). A 1.2 volt option will allow additional power and performance optimizations.
- SD8.0 defines full size SD supporting PCIe 4.0 x1 using the same form factor as defined for SD7.0 cards shown in Figure 3, plus SD Express cards with dual PCIe lanes using a third row of pins as shown in Figure 4. For dual lane cards, in order to extend the current consumption capability, an additional pin 19 was added as a second pin for VDD1 (3.3v). Pin 18 is reserved as optional 1.2v supply planned for future use allowing additional power and performance optimizations.

Figure 5 shows the bit rate performance levels of SD Express:

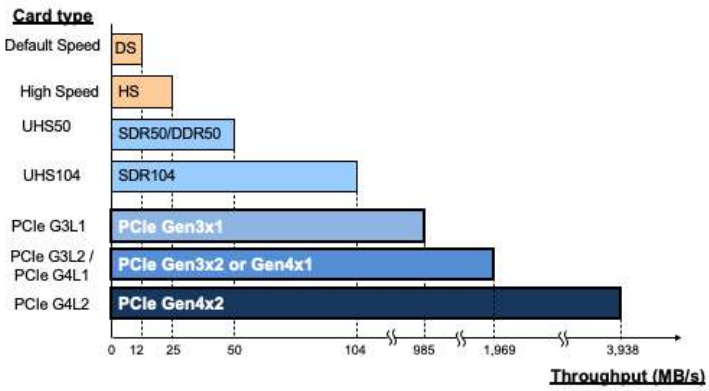


*Figure 5 - Bit rates for SD Express memory cards*

The SD Express interface and initialization process is flexible, allowing an SD Express compatible host to initialize the card through either legacy SD interface, or PCIe interface. The initialization through SD legacy is highly recommended, since it allows advanced notice about the card's capabilities and saves redundant re-iterations of non-supported card or protocol.

SD Express introduces itself to SD Express host as "Standard NVMe device" (Mass Storage controller→Solid State Controller→NVM Express device). Therefore, standard PCIe and NVMe drivers may access the SD Express card.

SD Express cards based on single lane PCIe 3.1 may consume up to maximum of 1.80 Watts from the host, representing the accumulated wattage from the two power supplies.

The following SD protocol features are supported partially by the PCIe and NVMe interface, assuming use of NVMe version 1.3. In the future, NVMe may fully support these features:

- **Password Lock/Unlock:** A card may be password locked/unlocked only through the legacy SD interface. The locked card does not allow access to the memory neither through the SD nor through the PCIe and NVMe interface.
- **Write Protect features:** A card may be set to write protected mode through legacy SD interfaces. A write-protected card does not allow any write operation to it neither through its SD nor through the PCIe and NVMe interface.

The following traditional SD features are not supported through the PCIe interface:

- SD CPRM Security: If the SD Express host accesses card through the PCIe interface that includes CPRM encrypted files, it will read them as encrypted data, which is the same result when inserting the card to any SD host that does not support CPRM.
- Speed Classes: Speed Class, UHS Speed Class and Video Speed Class are not supported or necessary through the PCIe interface.

## New Options for System Developers

PCIe and NVMe standards are highly capable protocols enabling various features and choices for system implementers to use. Here are a few examples of potential usage of PCIe and NVMe. Note that the given capabilities are not related to SD Express but to the nature of PCIe and NVMe capabilities.

**Bus Mastering**

- Bus mastering (first-party DMA) is natively supported in PCIe, see Figure 6.
- This feature allows inter-chip communication between devices.
- For example, a modem can send IO requests directly to the storage without any "help" from the Application Processor (AP):
  - AP can move to low power mode and save overall battery life
  - Better latency path from modem to storage device

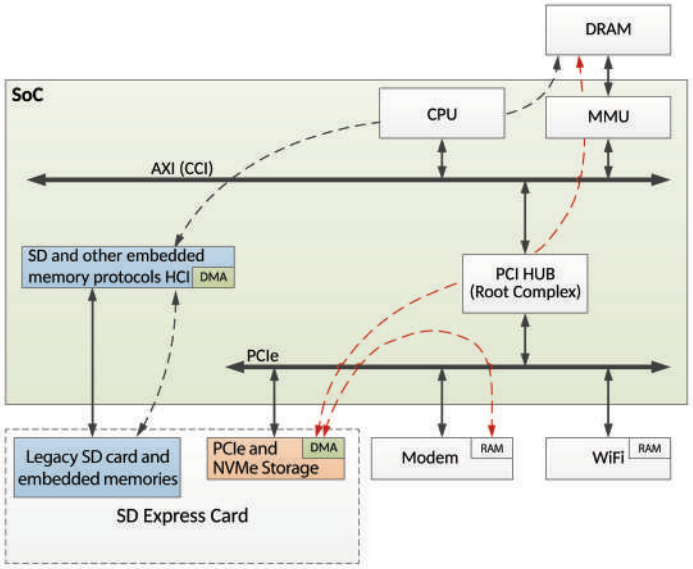


*Figure 6 – Bus mastering of PCIe*

**Multi Queue Support, Without Locking Mechanism**

NVMe can have a dedicated command queue in DRAM for every CPU core, see Figure 7.

- Other legacy embedded memory interfaces have one command queue in the Host controller.
- Synchronization and locking are needed in legacy protocols to mutually access the single queue.
- Legacy interface's host controller is a system bottleneck in the architecture.

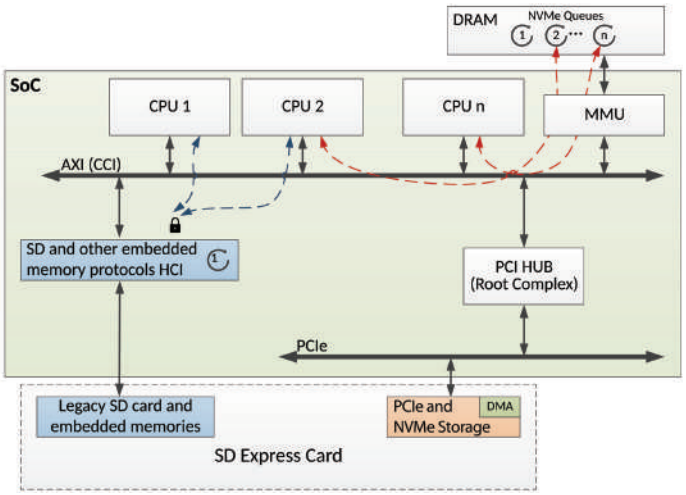


*Figure 7 – Host controller synchronization lock vs. Multi Queue support of NVMe*

**Host Memory Buffer (HMB)**

- High performance architecture usually requires extra controller resources. For example, embedded SRAM which is quite expensive compared to DRAM, see Figure 8.

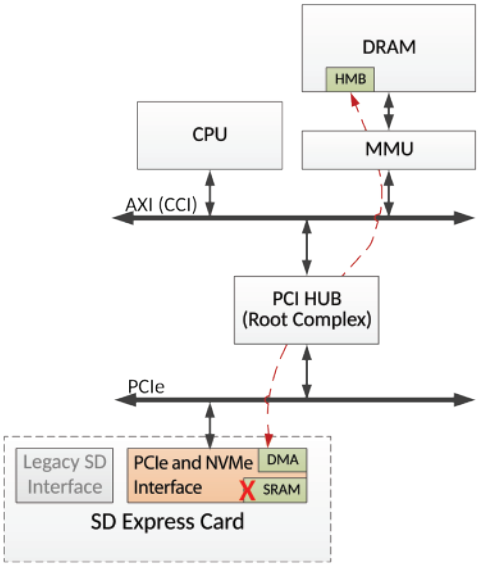


*Figure 8 – Host memory buffer description*

- HMB and Bus Mastering, native NVMe and PCIe features, are most useful in significantly improving storage performance with limited overall cost penalty. This is accomplished by using host DRAM resources as direct extension of controller internal RAM.
- The allocated DRAM size is subject to host device policy.
- Important: In the future, as SD Express becomes even faster, the use of the DRAM vs. SD card's memory may become system flexible. Instead of using the host's DRAM by the card saving card's SRAM, the SD Express card may become an extension of the host's DRAM, using the fast SD Express flash memory as the host's resource, saving DRAM.

## Tips for Host Product Manufacturers

With the use of the PCIe and NVMe interfaces, host product manufacturers can now consider using existing SD interface and PCIe and NVMe building blocks to utilize the new SD Express host interface development.

The only challenge with this design is the switching mechanism control of the shared signals – REFCLK, CLKREQ# and PERRST# with the legacy SD DAT lines. A straightforward solution is using an analog switch for these four lines controlled by VDD2 On/Off serving as SD/PCIe mode selection line (refer to Figure 9). Refer to the SD Express Host Design Guide for further information on how to implement SD Express host utilizing existing PCIe IP and SD Host controller with minor updates.

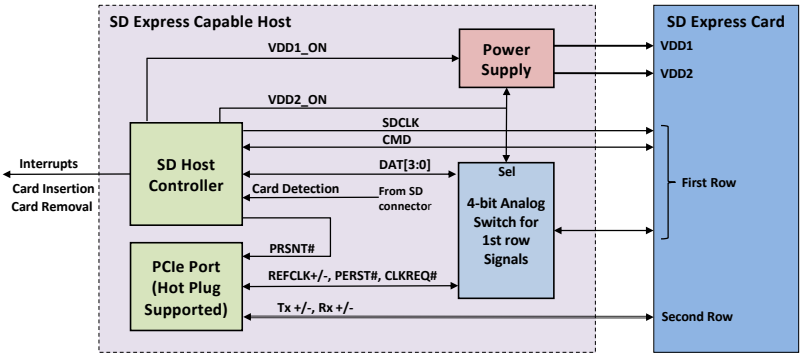


*Figure 9 – Example of SD Express Implementation*

Off-the-shelf solutions for combining existing PCIe and SD interfaces on the host side are readily available in the marketplace.

## Consumer Impact

Consumers will continue matching the card to their product for best performance. Manufacturers will use SDA symbols and logos on the product, its packaging and in the owner's manual). All SDHC, SDXC and SDUC memory cards with SD Express will have SD UHS-I interface and symbols allowing read and write operation on legacy SD interfaces. However, in order to reach maximum performance using its PCIe and NVMe interfaces, the host must support SD Express. Therefore, matching the SD Express host to and SD Express card is required to enjoy the best performance and the best user experience.

In Figure 10, the SD Express marking are as follows:


*Figure 10 - Various combinations of host and card marks*

Note that SD Express cards featuring PCIe 4.0, or dual lane cards, were not marked with specific symbol except their SD Express marking.

The PCIe standard supports full backward compatibility and interoperability between the various PCIe generations; therefore, a PCIe 4.0 card will operate in any PCIe 3 host and vice versa, including dual lanes. In other words, after the negotiation completes during the PCIe link up process, any type of SD Express card will operate in any type of SD Express host using its highest discovered common denominator automatically.

Regardless of the assured PCIe operation compatibility, it is highly recommended that hosts and card manufactures communicate to their customers the capabilities of products – i.e. PCIe generation (PCIe 3 or PCIe 4) and number of lanes supported on users manuals and packages. Or, alternately, the maximum supported byte rate. Such information would eliminate consumers' confusion when deciding to purchase the latest and greatest cards for host applications that are limited to lower generation specification or limited number of lanes.

Card types and expected maximum performance capabilities are outlined in Figure 11 and Figure 12.

| Host Type / Card Type | SD (any up to UHS50) | SD UHS104 | SD-UHS-II | SD Express |
|---|---|---|---|---|
| SD – up to UHS50 | Up to 50MB/s | Up to 50MB/s | Up to 50MB/s (basic SD interface) | Up to 50MB/s (basic SD interface) |
| SD UHS104 | Up to 50MB/s | Up to 104MB/s | Up to 104MB/s (basic SD interface and if host support it) | Up to 104MB/s (basic SD interface and if host support it) |
| SD-UHS-II | Up to 50MB/s | Up to 104MB/s (if supported by card) | Up to 156MB/s (Full Duplex) Up to 312MB/s (Half Duplex) | Up to 104MB/s (basic SD interface and if host support it) |
| SD Express | Up to 50MB/s | Up to 104MB/s (if supported by card) | Up to 104MB/s (basic SD interface and if host and card support it ) | See Figure 12 |

*Figure 11 Maximum performance of SD Express and standard SD host and card combinations*

| Host Type / Card Type | SD Express Gen3x1 | SD Express Gen3x2 | SD Express Gen4x1 | SD Express Gen4x2 |
|---|---|---|---|---|
| PCIe G3L1 | Up to 985MB/s | Up to 985MB/s | Up to 985MB/s | Up to 985MB/s |
| PCIe G3L2 | Up to 985MB/s | Up to 1,969MB/s | Up to 985MB/s | Up to 1,969MB/s |
| PCIe G4L1 | Up to 985MB/s | Up to 985MB/s | Up to 1,969MB/s | Up to 1,969MB/s |
| PCIe G4L2 | Up to 985MB/s | Up to 1,969MB/s | Up to 1,969MB/s | Up to 3,938MB/s |

*Figure 12 Maximum performance of SD Express host and card combinations*

# Summary

With SD memory cards used for higher capacity as well as speed intensive applications and massive storage for devices of all types, there is a growing need for a big jump in random and sequential performance levels as well as more modern protocols. The SD Express feature introduced initially in SD7.0, along with microSD Express in SD7.1 and then further enhanced in SD8.0, includes the added PCIe/NVMe interface beside the existing SD interface. Usage of PCIe and NVMe makes adoption easier thanks to leveraging existing knowledge by using given building blocks and available test equipment.

New cards successfully balance enabling a new world of usage opportunities for SD memory cards while keeping backward compatibility to billions of existing SD host. The microSD Express extends the opportunities for high speed applications by using the world's most popular removable card form factor of microSD. The newly introduced SD8.0 with bit rates of up to 2GB/s and 4GB/s will open even more opportunities for extra high performance solutions of removable memory cards leveraging the globally known and popular SD size form factor.