SD Express (SD7.x-SD8.0)
Host Implementation Guideline – Version 2

Design Guide | May 2025

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1. Purpose and Scope

The SD Association (SDA) introduced SD Express via the SD7.0 and microSD SD7.1 specifications followed by further speed increases in SD8.0 in anticipation of new market demands for high performance applications such as mobile computing, gaming and Internet of Things (IoT) as well as opening new opportunities for removable memory cards usage. SD Express integrates PCIe/NVMe interface to the legacy SD interface for SD and microSD memory cards while maintaining full backward compatibility.

The SDA prepared this document to provide recommendations on how to implement SD Express into host products to maximize the specifications capabilities of the new PCIe/NVMe interface and remain backward compatible.

The solution provided is intended for the adoption of SD Express support in chipsets. There are several off-the-shelf bridge solutions from either PCIe or USB3 to SD Express, that can be used for adding support of SD Express interface to any products that have a redundant PCIe or USB3 interface. More on those off-the-shelf solutions may be found in this video and webinar slides.
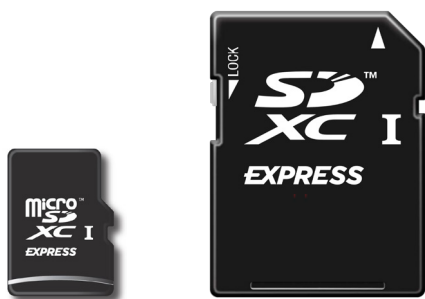
Figure 1 microSD Express and Full Size SD Express Cards

1.1 Referenced Documents

1.1.1 SDA Specifications:

- Part 1 Physical Layer Specification Ver 7.0 (SD Express full size introduction) referred to hereafter as SD7.0 and its Standard Size Mechanical Addendum Ver 7.0.
- Part 1 Physical Layer Specification Ver 7.1 (microSD Express added) referred to hereafter as SD7.1 and the microSD Card Addendum Ver 7.0.
  Note: When SD7.x specification is mentioned, it relates to both SD7.0 and SD7.1.
- Part 1 Physical Layer Specification Ver 8.0 referred to hereafter as SD8, its Standard Size Mechanical Addendum Ver 8.0 and the microSD Card Addendum Ver 8.0.
- Part A2 Standard Host Controller Ver 7.0 – Referred also as SHC.

Note that only SDA members and host or card licensees may obtain access to the official SDA specifications. In order to become a member – please refer to this link.

The SDA also published simplified versions of the specifications mentioned above that non-members may download for general study usage or driver development. The simplified specifications are not intended for product (card or host) development. Physical Layer Simplified Specification Ver 7.1 or newer can be downloaded from the following link.

1.1.2 PCI-SIG Specifications

- PCI Express Base Specification Revision 3.1a

PCI-SIG specifications may be downloaded from PCI-SIG site through this link.

2. SD Express Card – Description

A general comment about SD8 vs SD7.x – While SD7.x includes a single PCIe Gen3 lane, SD8 specification added the following interface configurations - PCIe Gen3 x2, Gen4 x1 and Gen4 x2. All the sideband signals are the same as in SD7.x. For the sake of simplicity, this document relates to SD7.x; however, the proposed solution concepts stay exactly the same for SD8. The only difference would be the number of supported TX/RX lanes and their speed.

SD Express and microSD Express memory cards are based on SD Physical spec Ver 7.0 and 7.1, respectively. For simplicity's sake, we will refer to them both as SD Express hereafter. All SD Express cards have the same general block diagram, as shown in Figure 2 while the only difference for SD8 might be an additional set of RX/TX lines.

SD Express Card Block Diagram

(*) The Bi-Directional Mux shown is just a functional description. The actual implementation may vary.
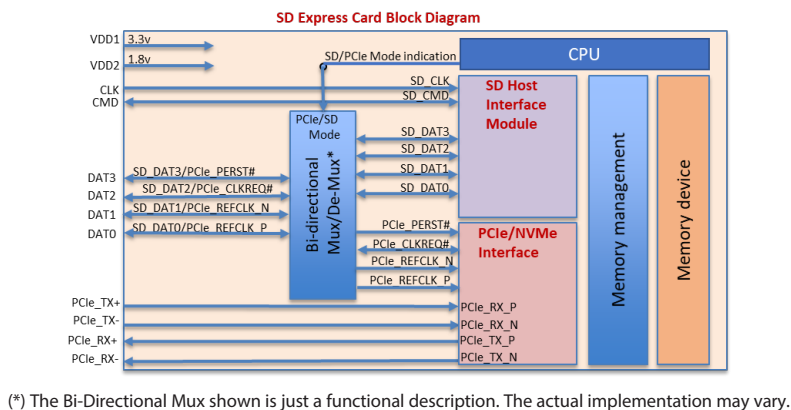
Figure 2 SD Express Card Block Diagram

To simplify the concept, an SD Express card can be considered a traditional UHS-I memory card with the PCIe interface and NVMe protocol.

The physical interface:
- The PCIe physical interface of SD7.x is as defined by PCI-SIG: PCIe 3.1 specification, single lane.
- The SD Express adopted the PCIe 3.1 spec using the following side band signals: PERST# and CLKREQ#.
- Power Supply of VDD2 = 1.8v (in addition to VDD1=3.3v) is mandatory for the PCIe interface to operate.
- Due to the limitation of space, the two side band signals and the REFCLK signals are muxed with the SD DATA lines.

The functional interface:
- In PCIe mode of operation, the card introduces itself to the host as a standard "NVM Express Device" (PCIe Class ID: 01h->08h->02;h as shown in PCI Code ID spec). This is the same as other NVMe devices like SSD or M.2 devices, so standard PCI/NVMe drivers can be used to access the card in PCIe mode.
- SD Express card may be initialized either through the SD interface or through the PCIe interface. The card may automatically recognize the PCIe mode of operation upon VDD2 supply from the host.
- If a host operates in PCIe mode, it may either:
  A. SD First: Initialize the SD Express card through the SD interface first after power up of VDD1 to check if the card supports PCIe. If it supports PCIe, it will switch to PCIe mode by supplying VDD2,
  B. Access the card directly in PCIe mode right after power up of VDD1 followed by VDD2. The card detects automatically that it is accessed with the PCIe interface and will operate as a standard NVMe memory device.

Bottom line: Implementation of SD Express host is simple, because:
1. Existing PCIe and SD interfaces may be utilized as-is and the existing SD interface, with minimal addition, may be used.
2. A relatively simple hardware mux/de-mux unit needs to be added at the front end allowing the separation of the PCIe side band and REFCLK signals from the SD DAT lines. There are readily available, off-the-shelf, dedicated units designed to perform mux/de-mux in the market today, making implementation easy.
3. As for software drivers, existing PCIe/NVMe drivers may be used. The only addition needed is the switching mechanism between SD drivers to PCIe and the control of VDD2 supply for PCIe mode of operation that may be used also as the SD/PCIe mode selection for the front end mux circuit. The SD drivers will require an update to support the new interface. That update is expected to be contributed to the open source community (see the drivers section below).

3. SD Host Types That May Accept SD Express Card

Any of the following hosts can use SD Express cards:

1. Host supporting both SD and PCIe interface:
- Host and card can use either SD or PCIe interface operating the SD Express card in either SD mode or PCIe mode.
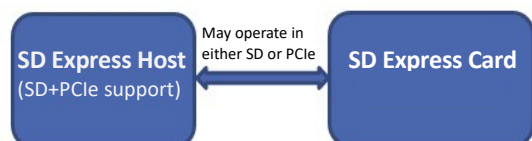
Figure 3 SD Express Host = SD and PCIe

2. Host supporting only SD interface:
- Host and card will use SD pins operating the SD Express card in SD mode.
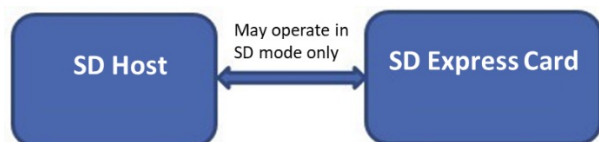
Figure 4 SD UHS-I Host

Important: Note that the SD Express cards support either the SD UHS-I interface or PCIe/NVMe interface. A host, however, may be designed in a way, to support all types of interfaces: SD UHS-I, SD UHS-II and PCIe/NVMe. Currently, there are several PCIe or USB to SD Express bridge chips that support **all** three types of SD interfaces. More information on these off-the-shelf solutions are available in this video and this webinar. Note, the generic solution example presented in this document only supports SD UHS-I and SD Express cards (not UHS-II).

3. Host supporting only PCIe interface:
- Host only supports SD Express card
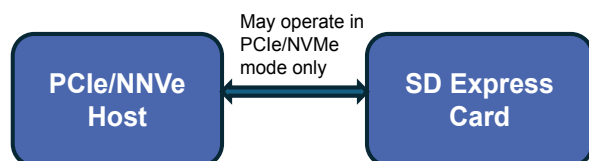
Figure 5 PCIe/NVMe Host

SD Express cards may be fully operated through its PCIe interface as a standard NVMe memory device using the standard PCIe/NVMe drivers on the host. However, a host only supporting the PCIe/NVMe interface is not backward compatible with legacy SD memory cards. Therefore, the SDA would recommend avoiding such solutions unless it is used during the product development process (e.g., using M.2 to microSD Express adapter) as described in section 3.3 or after the various concerns mentioned below were considered.

Hosts have the option to use an interface that supports only PCIe/NVMe and use SD Express cards operating standard PCIe/NVMe drivers. However, the host will not be able to operate any standard SD memory card (UHS-I). Such a design might confuse consumers who try to insert standard SD memory cards. Therefore, it would be recommended to avoid this option, especially in the case of the potential use of standard SD memory cards, not to mention that such a solution might not comply with the SD Host Licensing provided by 3C LLC. Hosts that choose to implement a PCIe/NVMe-only host, may not use the SD trademarks.

Figure 6 The SDA's Express Mark Defined by the SD Association

The SDA's Express mark may be used if the host vendor is an SDA member, otherwise, the word "Express" may be used along with clear instructions for consumers that only SD Express cards may be used with this interface. The SDA recommends such uses be limited to semi-embedded installations whereby these cards are installed under cover or other product-specific related cards to minimize consumers' attempts to use a standard SD memory card in the host. Such an operation option is described in Section 3.2.

3.1 SD Express Host

3.1.1 Pin out
- SD 7.0: Refer to Table 3.7.3-1 of SD7.0 Specification.
- microSD 7.1: Refer to Figure 2-4, and Table 2-5 of microSD Card Addendum Ver 7.10 Specification.

3.1.2 Recommended Features
Refer to Section 8.1.3 to 8.1.6 of SD7.0 Specification for SD 7.x card supported, optional, not supported, and partially supported features. SD 7.x Host is highly recommended to support at least all SD 7.x card supported features (Section 8.1.3 in SD7.0) on host side.

When designing an SD Express host product, consider the following recommendations to best utilize SD Express card capabilities.

SD Mode:
- Allow maximum power in default speed mode of SDXC and SDUC cards by setting power control bit in ACMD41, XPC, to 1 as this is the maximum performance mode.
- Send Power off notification to the card before turning OFF the power to the card during idle time.

PCIe Mode:
- The SD Express PCIe interface uses CLKREQ# and PERST# sideband signals only. The initialization process/conditions should conform to the PCIe and SD Express standard.
- Support Single Lane (x1).
- Support hot pluggable feature.
- Host should allow SD Express card to work in full swing operation mode (800mV) even though PCIe allows full swing operation and half swing operation.
- Host should support the latest available NVMe 1.3+ (e.g., 1.3d at the publication of this document) to assure full backward compatibility and interoperability to all cards in the market.
- Support up to 1 namespace.
- L1.1 and L1.2 power sub-states to be supported in PCIe for power saving during standby.
- Host may manage power and thermal conditions using the card's three power states: 0.72W, 1.44W and 1.8W (default) through the NVMe protocol.

3.1.3 Interface Detection and Initialization Sequence
Refer to Section 3.17.2 in SD7.x for the initialization sequence shown from host and card sides that cover all the cases. A more detailed description of each specific case along with signal diagrams can be found in Section 8.3.2 of SD7.x.

3.2 SD Host
Any legacy SD host in the market may support the operation of an SD Express card. In such a host, the SD interface of the SD Express card will be used as guaranteed by the specification. Speeds of SDR50 and DDR50 for microSD Express will be supported while DDR50 in full size cards and SDR104 may also be supported if implemented by the cards.

Refer to Section 3.17.2 in SD7.0 Specification for the SD Express card internal state diagram. Initializing the card with legacy SD host will move the card to its SD mode of operation at the moment that SD CLK will be provided by the host.

3.3 PCIe Host

3.3.1 Interface Selection and Pin out
- As mentioned earlier, the SDA is not recommending implementation of PCIe host that does not support SD, as this host will not be backward compatible to existing legacy SD cards.
- There is no issue to operate SD Express cards in PCIe host because it supports initialization directly through the PCIe interface. Therefore, it can be used in such ways for non-retail usage and for the development process.
- A standard PCIe 3 interface may be used on the host side with the following considerations:
  - Side band signals used with SD Express card are PERST# and CLKREQ#.
  - Card Present Detect (PRSNT#) input shall be supported (as should be provided by any PCIe interfaces supporting hot plug in/out).
  - In order for the SD Express card to operate in PCIe mode, it needs VDD1 (3.3v) and VDD2 (1.8v) power sources to be supplied plus VDD2 must be supplied to the SD Express card after VDD1 is set to ON.
  - SD Express card does not have internal AC coupling capacitors on its PCIe output lines. The two AC caps (176nF to 265nF as defined in PCIe standard)

need to be added on host within a distance of up to 12.5mm from the SD connector's PCIe RX lane contacts. Those caps are in addition to the AC coupling caps already connected at the output of the PCIe lines of the host side.

- Refer to Section 3.7.3 and Table 3.7.3-1 of SD 7.0 Specification for SD form factor pin out.
- Refer to Section 2.4 and Table 2-5 of microSD Card Addendum Ver 7.1 Specification for microSD pin out.

3.3.2 M.2/PCIe to SD 7.x Card Adapter

A practical example of PCIe Host usage for test and/or development of PCIe interface of SD Express card may be done through a M.2/PCIe Card to SD Express card adapter. Such a solution may allow the operation of SD Express card in existing host that includes PCIe card or M.2 card slot. Figure 7 shows an example adapter card.
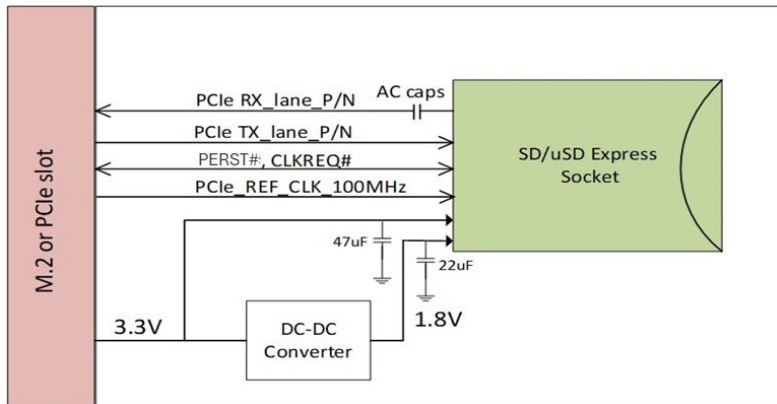
Figure 7 M.2/PCIe to SD7.x Adapter

Note that the 1.8V can be derived from 3.3V on the adapter board using DC-DC converter as shown above (optional). The 1.8V supply must be delivered to the card after the 3.3V supply is on. In addition, two AC caps need to be added, one to each signal line of the RX lane close to the SD Express connector (the card does not include them) as described also in section 4.1.

3.3.3 Interface Detection and Initialization Sequence

Refer to Section 3.17.2 in the SD7.0 specification for the initialization sequence shown from the host and card sides that covers all the cases. Use the PCIe direct path, not through the SD interface, first. For the configuration shown in Figure 7, the host may use the existing standard PCIe/NVMe initialization process and drivers. The card, as mentioned, will conform to PCIe specification and introduce itself as a standard NVMe memory device.

3.3.4 Recommended Features

- SD Express host initialization process and conditions should conform to the PCIe specification.
- The host should support up to PCIe Gen 3.1 with up to 985 MB/s and CLKREQ# + PERST# side band signals.
- Support Single Lane (x1).
- Support hot pluggable feature.
- SD Express host should allow SD Express card to work in full swing operation mode (800mV).
- Host should support the latest available NVMe 1.3+ (e.g., 1.3d at the publication of this document) to assure full backward compatibility and interoperability to all cards in the market.
- Support 1 namespace.
- L1.1 and L1.2 power sub-states to be supported in PCIe for power saving during standby.
- Host may manage power and thermal conditions using the card's three power states: 0.72W, 1.44W and 1.8W (default) through the NVMe protocol.

Note: An SD Express host is not required to recognize an inserted SD Express card. As mentioned, the card appears as a standard NVM Express device. However, in cases where the host is aware of the existence of SD, and it wants to read some of the unique SD registers information, it may access it through some of the NVMe registers. For further information, refer to Section 8.1.7 of SD7.0 Specification for register mapping SD→NVMe/ PCIe.

4. Hardware

4.1 SD and PCIe Host Interface with SD Express Socket

This section provides an overview of how a host may utilize an existing SD host controller and existing PCIe interface to implement the interface necessary to support SD Express cards.

The PCIe interface used in SD Express card includes the following three signal groups:

1 Differential interfaces:
   - PCIe_TX_P and PCIe_TX_N – Inputs to the card
   - PCIe_RX_P and PCIe_RX_N – Outputs from the card
2 Differential CLK Interface:
   - PCIe_REFCLK_P and PCIe_REFCLK_N – Inputs to the card
     These lines are muxed in the card with DAT0 and DAT1 of the SD interface
3 Sideband Signals:
   - PERST# – logic output from host to the card, muxed in the card with DAT3 of the SD interface
   - CLKREQ# – Open drain I/O for both card and host with pullup on host side, muxed in the card with DAT2 of the SD interface

In addition, there is a VDD2 (1.8v) supply to the card that is required only for the PCIe mode. A possible solution is to use an existing PCIe host module and existing PCIe/NVMe drivers along with minimum changes in the SD host controller with an added analog switch for the front end. This is recommended by SDA and described in the next paragraph. Note that there are other solutions allowing use of existing circuitry of PCIe interface from different vendors available in the marketplace today. An example of this off-the-shelf solution is provided in Appendix C.

The SD Express interface was defined in a way that existing PCIe IP (supporting hot plugin) and SD host controller V3 may be used to implement the SD Express interface with minimal additions. The only challenge

on the host side would be the handling of the switched signals. There are many ways to implement such switching considering the nature of the combined signals, especially if it is implemented within a SoC. In this document a straightforward example of Bi-Directional Analog Mux is shown. Any type of solution that meets the SD Express interface requirements is correct.
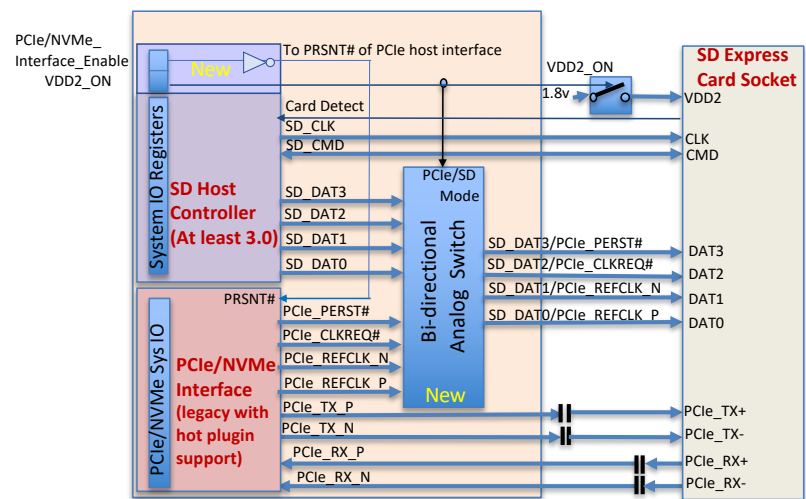
Figure 8 SD Express Host – Block Diagram

The block diagram example of an SD Express host in Figure 8 shows a case in which host vendor, or chipset vendor, utilizes the existing PCIe host IP that supports hot plugin with card presence detect PRSNT# input and SD Host Controller with at least SD Host Controller (SHC) V3 specification interface and minimal addition of two new control registers to implement a unified SD Express card interface.

The Bi-Directional Analog Switch shown is a functional representation of various possible practical solutions that may be implemented. Its functionality is to do the switching between SD_DAT(3:0) lines and the side band signals + PCIe REFCLK, allowing a single functionality, at a single time, towards the SD Express card – either as PCIe or as SD. It is assumed that the PCIe/SD functionality is selected through a control line.

The VDD2 line supplied to the SD Express only for PCIe operation mode may be used to switch the analog switch to PCIe mode. Note that the PCIe/SD Mode control signal, used for the switch, and VDD2 may be implemented as separate control lines; however, it may be simplified if VDD2 is used for the front end PCIe/SD mode selection (see example as well as the initialization flow charts shown in Section 5).

The Card Detection Mechanism in Figure 7 shows an existing SD socket card detect switch connected to an existing SHC and the card presence detect of the PCIe interface (PRSNT#) is connected to the output of the new SHC register (controlled by a new PCIe/NVMe_Interface_Enable bit), allowing overall control of the driver's operations through the SD drivers. Detailed description of new control bits of registers (VDD2_ON, PCIe/NVMe_Interface_Enable and PCIe/NVMe support) is provided in Section 4.1.1 below.

Figure 7 describes the SD Express Host connections with emphasis on the new control lines and ability to perform the switching between SD and PCIe modes with their associated driver's usage. A detailed flow chart of the updated SD drivers that can support the given example is shown in Section 5.4.

Figure 9 Block Diagram of SD Express Host with New Control Lines

Figure 10 shows a straightforward example of usage of external discrete component serving as Bi-Directional Analog Switch. Any type of solution that will meet the SD Express interface requirements is acceptable.

Figure 10 A Practical Example of Mux/De-Mux Circuit

The following are a few hardware considerations when implementing the above example:

- Parasitic capacitance of the multiplexer device should be considered while selecting the multiplexer device and designer should make sure the design meets the SI requirements like jitter, insertion loss, etc. for SD/PCIe interface as per SD Express specification.
- To support hot insertion of SD Express cards, host product design should provide enough capacitance on host board on both VDD1 and VDD2 power rails to reduce influence of voltage drop caused by hot insertion. See Appendix E Host PDN Design Guide of *SD 7.0 Specification* for more details.
- Figure 10 shows a typical host board design circuit used in a host product with an SD interface and PCIe interface separated, along with external components for the front-end SD Express.

- The given components such as the analog switch are provided as an example for reference only. It is the implementers responsibility to meet all the interface electrical characteristics as defined in SD Express specification.
- Updated SD drivers should take care of the selection between the modes of operation by enabling/ disabling of VDD2 supply and providing indication to the PCIe host unit about card insertion/removal.
- AC caps value can be from 176nF to 256nF for PCIe Gen3 speed and these caps must be placed very close to SD Express socket (< 12.5mm from Socket).

4.1.1 Proposed Additions to SD Host Controller – In Detail

Additions to existing SD Host Controller that enable the solution shown in Figure 8 are given below. Figure 11 shows the lower range of the SD Host Controller Register Map (as provided in detail in the SD Host Controller Specification available for SDA members on the SDA Website). The newly proposed register bit loca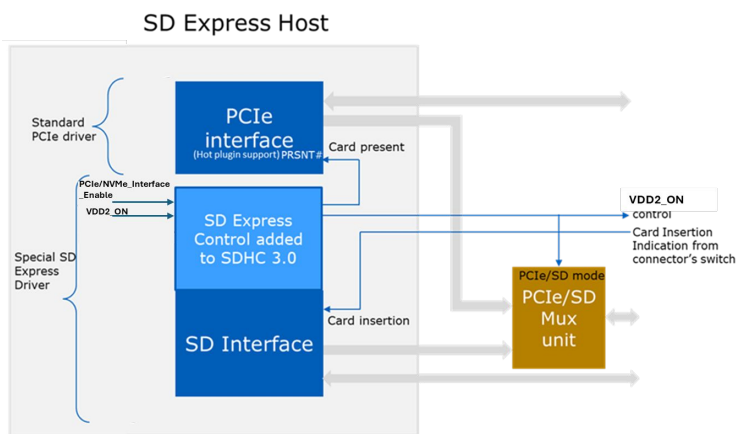tions dedicated to SD Express are shown in Figure 9 as well. Additional details on the added register bits are as follows:

- **VDD2_ON:** Support of VDD2_ON was introduced in SHC V4.0 (originally dedicated for the UHS-II interface) and is described in the Power Control Register, mapped as bit D04 in offset 29h. The same control bit may be used for SD Express card. Turning on this bit will connect VDD2 supply to the card as well as set the front end Analog Switch in the host to PCIe mode.
- **PCIe/NVMe_Interface_Enable:** A new register area is used for this new control bit – mapped as bit D00 in offset 55h. This bit, if set to "1," will assert PRSNT# (to "0") line connected to the PCIe host interface. The PRSNT# line is available in PCIe host interfaces that support hot plugin used originally as indication for card insertion. Therefore, assertion of PRSNT# tells the PCIe drivers to take control and start to initiate the card using the PCIe interface. The same way, if PCIe/NVMe_ Interface_Enable bit is set to "0", PRSNT# is de-asserted (to "1") which will indicate to the PCIe host interface and drivers about card removal.
- **SD Express Support Indication:** Allowing the updated SD drivers to know whether the given SHC supports SD Express interface in the Capabilities Register will be updated to include a new bit indicating PCIe/NVMe Interface support – mapped as bit D20 in offset 40h. If this bit indicates "1" (supporting SD Express) then bit 1.8V VDD2 Support (D60) in Capabilities Register is set to "1" as well.

Offset	15-08 bit	07-00 bit	Offset	15-08 bit	07-00 bit
002h	32-bit Block Count (High) SDMA System Address (High)		000h	32-bit Block Count (Low) SDMA System Address (Low)	
006h	16-bit Block Count		004h	Block Size	
00Ah	Argument (High)		008h	Argument (Low)	
00Eh	Command		00Ch	Transfer Mode	
012h	Response1		010h	Response0	
016h	Response3		014h	Response2	
01Ah	Response5		018h	Response4	
01Eh	Response7		01Ch	Response6	
022h	Buffer Data Port1		020h	Buffer Data Port0	
026h	Present State		024h	Present State	
02Ah	Wakeup Control	Block Gap Control	028h	Power Control	Host Control 1
02Eh	Software Reset	Timeout Control	02Ch	Clock Control	
032h	Error Interrupt Status		030h	Normal Interrupt Status	
036h	Error Interrupt Status Enable		034h	Normal Interrupt Status Enable	
03Ah	Error Interrupt Signal Enable		038h	Normal Interrupt Signal Enable	
03Eh	Host Control 2		03Ch	Auto CMD Error Status	
042h	Capabilities		040h	Capabilities	
046h	Capabilities		044h	Capabilities	
04Ah	Maximum Current Capabilities		048h	Maximum Current Capabilities	
04Eh	Maximum Current Capabilities (Reserved)		04Ch	Maximum Current Capabilities (Reserved)	
052h	Force Event for Error Interrupt Status		050h	Force Event for Auto CMD Error Status	
056h	---		054h	Host Control 3	ADMA Error Status
05Ah	ADMA System Address [31:16]		058h	ADMA System Address [15:00]	
05Eh	ADMA System Address [63:48]		05Ch	ADMA System Address [47:32]	
062h	Preset Value		060h	Preset Value	
066h	Preset Value		064h	Preset Value	
06Ah	Preset Value		068h	Preset Value	
06Eh	Preset Value		06Ch	Preset Value	
072h	---		070h	---	
076h	---		074h	Preset Value for UHS-II	
07Ah	ADMA3 ID Address [31:16]		078h	ADMA3 ID Address [15:00]	
07Eh	ADMA3 ID Address [63:48]		07Ch	ADMA3 ID Address [47:32]	

VDD2_ON: Use existing bit register definition as appears in SHC ver 6.0 for "SD BUS Power for VDD2" (just change the bit description to: "VDD2 Power On")

PCIe/NVMe Support: Using reserved bit D20 in capabilities register to indicate SHC supporting SD Express. If this bit is set to 1, it also means **1.8V VDD2 Support** (D60) is set to 1

PCIe/NVMe_Interface_Enable: Define new register using this reserved area.

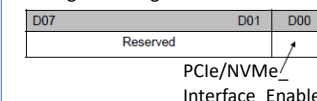| D07	D01	D00
Reserved		

PCIe/NVMe_ Interface_Enable

Figure 11 SD Host Controller Register Map with Added SD Express Support

4.2 Power Supply

Table 1 describes the voltage ranges and max current levels for SD Express card compliant to SD7.x in PCIe mode of operation. Note that in any case, the SD7.x card is not allowed to consume more than 1.80W in total. Note that SD 8 cards may consume higher power rates. Refer to the Standard Size Mechanical Addendum Ver 8.0 and the microSD Card Addendum Ver 8.0 for further information.

Power Rail	Voltage Range	Peak Current [Max Avg at 25usec (mA)]	Normal Current [Max Avg at 1sec (mA)]
VDD1 (3.3)	2.7 - 3.6V	600	400
VDD2 (1.8)	1.7 – 1.95V	600	400

Table 1 Voltage Ranges and Max Currents Allowed in SD Express Card Compliant to SD7.x at PCIe Mode

4.3 Hot Plug-in/Removal and Card Detection

The PCIe host should support hot plugin and removal. It is highly recommended to turn off the power supplies before card removal. An SD Express host should use the card detection switch of the connector as SD Express card presence detection mechanism, the same as used by the existing SD Host Controller. The card presence detection of the PCIe interface (PRSNT#) is connected to the output of SHC, allowing the SD drivers to inform the PCIe interface about card insertion/removal.

VDD2 shall be OFF while the card is inserted. VDD2 should be turned on only if PCIe interface is to be initiated and always only after VDD1 was turned ON. VDD2 is used to switch the front-end Analog Switch of the host to PCIe mode and is one of the factors that will trigger the card to switch into PCIe mode.

4.4 PCIe Differential Voltage Swing

Refer to *Section 8.2.2* of *SD 7.0 Specification* for differential voltage swing details.

4.5 PCIe REFCLK Guidelines

Refer to *Section 8.2.3* and *Table 8-3* of *SD 7.0 Specification* for REFCLK specification.

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(1) The listed sources are the companies known to the author at the publication date. Any other SDA members that supply such connectors are welcome to contact SDA office to be added in the provided list.

(2) The listed sources are the companies known to the author at the publication date. Any other SDA members that supply such connectors are welcome to contact SDA office to be added in the provided list.

4.6 PCIe Sideband Signals CLKREQ# and PERST# Guidelines

Refer to *Section 8.2.4* of *SD 7.0 Specification* for CLKREQ# and PERST# electrical specification.

4.7 PCIe AC Coupling Capacitors

Refer to *Section 8.2.5* of *SD 7.0 Specification* for A.C. coupling capacitors placement guidelines.

4.8 PCIe TX/RX PHY Protection

Refer to *Section 8.2.6* of SD 7.0 Specification for 3.3v IO tolerance on PCIe TX/RX PHY.

4.9 ESD Recommendations

Refer to *Section 6.8* of *SD 7.0 Specification* ESD Guidelines.

4.10 SD Express and microSD Express Connectors Suppliers

4.10.1 SD Express Full Size Card Connector

The SD Express pads layout/location is identical to UHS-II; therefore, any existing full-size SD UHS-II connectors that operate at the desired speeds will work. It is recommended to check with the connector vendors for availability and supported frequencies.

SDA members offering UHS-II connectors include:
- Amphenol ICC - https://www.amphenol-cs.com/product-series/sd-express.html
- Taisol - https://www.taisol.com/connector/card-reader/sd-conn/?lang=en_US
- V-General (SD7 and SD8) - https://en.v-general.com/products/941_942_979.htm
- Others[1]

4.10.2 microSD Express Connector

The microSD Express Card requires new connectors to be used because the location and size of the second row is different from the microSD UHS-II cards.

microSD Express (SD7.1) connector suppliers:
- Amphenol ICC - www.amphenol-icc.com/micro-sd-express
- Taisol - https://www.taisol.com/connector/card-reader/micro-sd-conn/?lang=en_US
- Others[2]

5. SW Drivers

Before discussing the actual drivers - a flow chart of two possible initialization processes as defined in SD specification is shown in a simplified manner. Figure 10 shows a case where the SD Express host initializes the SD Express card through the PCIe interface. If the initialization fails, it defaults to SD interface. Figure 11 shows a case where the SD Express host initializes the SD Express card first through SD interface, checking if the card supports PCIe then switches to PCIe mode.

These example flows are simplified to assume that PCIe and SD drivers can both be updated and may control the transfer of control to the other driver. It is shown just for the sake of understanding the general init flow. The solution provided in this document allows change **only** of SD drivers while keeping the PCIe drivers as is. The actual new flows that consider the proposed HW above are given in Section 5.4 below.
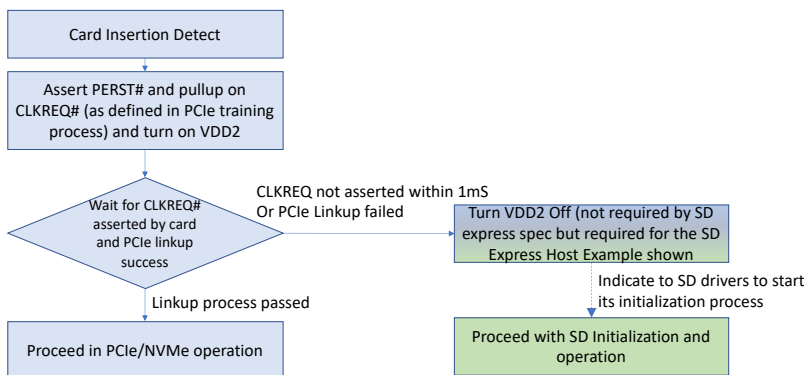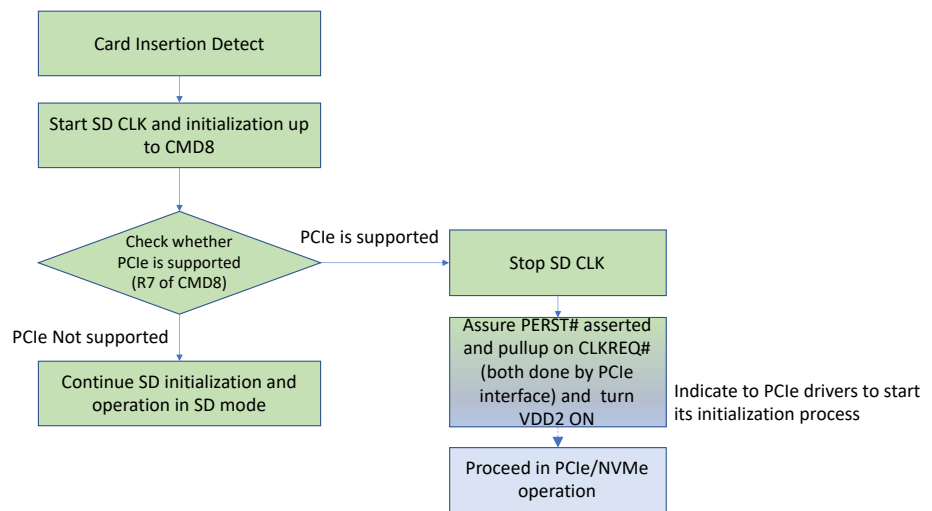

Figure 13 Flow Chart of Initialization Process Starts from SD Drivers First

As shown, SD Express host or chipset providers can use its existing PCIe and SD interfaces and combine them with front end circuitry that can be implemented either externally to existing SoCs or inside a future SoC. Regardless of the actual HW implementation, the host will need to update its SW drivers to support the new SD Express Interface. Assuming that the host supports standard PCIe and NVMe drivers the only required update is to the SD drivers as follows:

- Updated SD drivers supporting the new registers proposed for the SHC that detect the SD Express card type and perform the switch between the interfaces (controls the VDD2_ON and PCIe/NVMe_ Interface_Enable).
- In cases when the host does not support NVMe, add standard NVMe drivers above the PCIe, supporting a standard NVMe device interface.

Figure 12 Flow Chart of Initialization Process Starts from PCIe Drivers first

A description of the drivers layering in Android based system is shown in Figure 14.
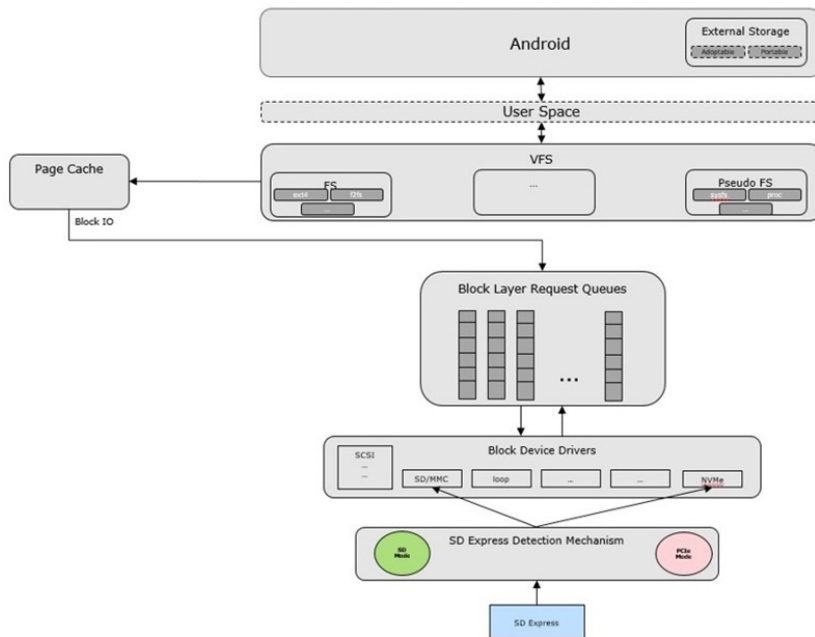

Figure 14 SD Express – Android Host Driver Layers Overview

References to existing NVMe drivers and SD are discussed in the following sections.

IMPORTANT: The proposed solution assumes usage of existing PCIe drivers (supporting hot plugin) while the SD drivers need to be updated to support the new init flow and switch control to/from SD/PCIe interface as shown in Section 5.4.

5.1 NVMe Drivers

Table 2 includes a list of a few available drivers for NVMe for the various operating systems as provided in http://www.nvmexpress.org/drivers/

Operating System	Driver Available
Chrome OS	Chrome OS
Linux	RHEL 6.5, 6.6, 6.7, 7.0, 7.1 SUSE 11 SP3, 12 Ubuntu 13, 14
Windows	Windows 7, 8, 8.1, 10 Windows Server 2008 R2, 2012, 2012 R2
UEFI	UEFI
UNIX	Free BSD Solaris 11.2 or higher
VMware	ESXi 5.5, 6.0

Table 2 NVMe Drivers

5.2 PCIe Drivers

Standard PCIe drivers providing hot plugin are supported by most of the OSs including Windows and Android (Linux/Kernel). The Linux drivers can be found in the standard Linux-Kernel code package: https://www.kernel.org/. The PCIe Hotplug support is part of the whole package and can be found in the following kernel file tree: *drivers/pci/hotplug/pciehp_hpc.c*.

Important security information related to the PCIe system:

The PCIe specification allows direct memory access (DMA) for any connected device on its network, including externally connected devices. PCIe hot plug devices such as Thunderbolt, USB4, CFexpress as well as SD Express allow users to attach classes of external peripherals, including graphics cards, to their devices with the plug-and-play ease of USB. These devices are DMA-capable and can access system memory and perform read and write operations without the need for the system processor's involvement. This capability is the reason behind the exceptional performance of PCI devices, but it also makes them susceptible to drive-by DMA attacks. This might introduce a vulnerability of the PCIe system if the system designer is not aware of it.

In PCIe, where the endpoint can access DRAM, the host should restrict the endpoint from accessing unauthorized/sensitive/secure areas. If the device has a bad firmware(FW) update mechanism and is injected with FW that could take advantage of it, or the card was originally manufactured to take advantage of it, then it could be a problem if the host does not limit the access privileges. Part of the reason Device Attestation standards exist is to limit such attacks and have the host know with whom it is communicating.

Most operating systems are now applying IOMMU-based restrictions for external PCIe devices.

For Android - https://source.android.com/docs/core/virtualization/architecture

For Windows - https://learn.microsoft.com/en-us/windows/security/hardware-security/kernel-dma-protection-for-thunderbolt

Those are examples of existing market solution tools provided to control and eliminate such potential vulnerability of the products.

Bottom line – this issue may be kept as a good and powerful feature, without being harmful for the SD Express interface, if care is taken by utilizing the same commonly used solutions already in place for all other externally attached PCIe hot plug devices.

5.3 Existing SD Drivers (for legacy cards)

Table 3 describes operating systems that support **existing** SD drivers for SHC v3.0. SD Express updated drivers will be required as described in Section 5.4. These new drivers are expected to be contributed to the open source community and hopefully adopted by Windows.

Mode	Linux Kernel Support	Windows Support	Android Support
SD	Kernel 2.6.20 onwards	Windows 7 onwards	Android version 1.5 (Cup Cake) onwards

Table 3 Existing SD Drivers

5.4 The New SD Drivers Functionality

As mentioned earlier, to support the SD Express Host example shown in Figure 9 only the SD drivers need to be updated, in comparison to the old SHC v3 drivers. Existing PCIe drivers that support hot plugin and standard NVMe drivers may be used as-is. Figure 15 below shows more detail of the init flow of the new SD driver. The green blocks relate to the SD driver and the blue to the PCIe drivers.

Note that fallback option (switch PCIe mode to SD mode) in both cases is not shown because it requires, for example, a special OS Sys application that tracks the PCIe initialization failure and provides the information to the SD drivers, and such information may not be provided directly from the standard PCIe drivers. This application is not defined because the fallback method relies on host system implementation.

Table 4 describes the advantages of one initialization process over the other.

Case# / Inserted Card	Standard SD Pros	Standard SD Cons	SD Express Pros	SD Express Cons
#1 SD-First	No delay in init	---	---	Few mS delay due to SDs 74clks+CMD0+CMD8
#2 PCIe-First	---	1ms of PCIe training OR Linkup time(in case that CLKREQ# ignored by host) + OS App time if needed*	No delay in Init	----

(*) If we assume no change in PCIe driver then external OS Sys App is required to monitor for PCIe failure and inform the SD driver
  The response time of such App is not so predictable, might take more significant time and therefore this option will not be discussed here

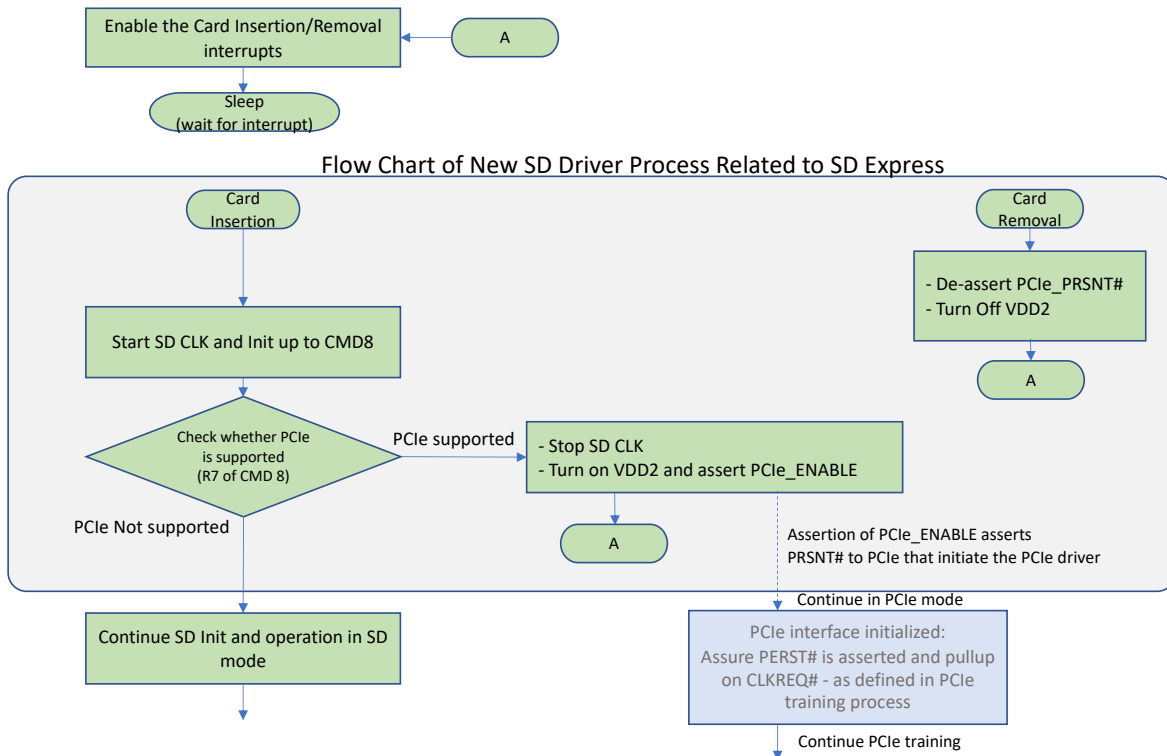*Table 4 Pros and Cons of Initialization Options: SD-First or PCIe-First*

Figure 15 Flow Chart of the Updated SD Drivers Operation During Initialization

Host vendors should be aware that this interface supports either legacy SD Memory Cards or SD Express cards. But for SD Express cards, there is no fallback to SD option proposed, even in the rare chance of a malfunctioning PCIe interface.

SDA recommends implementation of the SD-First option using an updated SD driver that can handle the switch between either SD mode or PCIe/NVMe mode. This prevents SD memory cards without the PCIe interface to go through the trial of PCIe and the subsequent, time consuming, re-tries. **As long as standard PCIe drivers are used – the option of SD-First (without fallback option) is both the safest and fastest solution.**

6. Power and Thermal Management

Power consumption affects two main aspects, Consumed Energy, or power over time, which impacts battery life; and thermal issues, arising from high power, generates heat that needs to be controlled and kept under the maximum allowed temperatures.

The following are the two main PCIe/NVMe features that should be used by the host to control the above two issues.

6.1 PCIe Power Management

PCIe interface supports several Power Modes (PM) that control the consumed power in idle state by setting internal various configurations of the differential interface as shown in Table 5. Each state might have different power vs. wake-up time characteristics.

For longer battery life, host should support L1.0 and its substates (L1.1 and L1.2) along with the control of CLKREQ# signal (as introduced by PCIe 3.1) for maximum power saving during idle mode.

Power Modes and substates	Port Circuit Power On/Off		
	PLL	Rx/Tx	Common Mode Keepers
L1.0	On	Off/Idle	On
L1.0+CLKREQ#	Off	Off/Idle	On
L1.1	Off	Off	On
L1.2	Off	Off	Off

Table 5 PCIe Power Substates

For more information, refer to the power management feature using L1.1 and L1.2 PM substates recommended in *PCI-SIG V3.1a Chapter 5.5.*

6.2 NVMe Power States

NVMe specification supports the Power States feature allowing the host to control the maximum consumed power by the card. SD Express specification defined three power levels supported by any SD Express card as following: 1.8W (default), 1.44W and 0.72W (Refer to *Section 8.1.8* in *SD7.x specification* for further information).

A detailed description of the Power States structure and usage by NVMe is provided in the *NVMe Specification, Section 8.4.*

For an SD Express card operating in SD mode, the same power levels (1.8W, 1.44W and 0.72W) are supported and controlled through the existing SD power modes control mechanism.

A SD Express host will use the NVMe power states for thermal management assuming that limiting the card's power consumption should reduce the card's case temperature. Refer to the thermal management feature in *Section 8.4.5 of the NVMe specification* for more information.

Card Power Consumption [W]	0.72	1.44	1.8
Max Card Case Temperature [degree °C]	87	80	75

Table 6 Card's Maximum Card Case Temperature (Tc) Allowed at Each Power State

Host needs to maintain card case temperature at a given power state as shown in Table 6 (as shown in Section 3.7 *of microSD Card Addendum version 7.1 and Section 3.6 of Standard Size SD Card Mechanical Addendum version 7.0*)

To utilize the best performance capabilities of the card, it is recommended for host vendors to conduct a full system level thermal simulation to arrive at optimized thermal design.

The following are some of the ways to counter thermal challenges:
- Host PCB/s design
- Heat pipe
- Graphene tape
- Connector design
- Heat sink and fan

This document includes some commonly used ideas for thermal solutions in Appendix A.

7. SD Express and microSD Express Test

Since SD Express is using a standard PCIe interface and introduces itself as a standard NVMe device, any standard off- the-shelf test equipment used for PCIe electrical and protocol tests and NVMe protocol tests may be used to test the PCIe/NVMe interface of the card side or host side.

SDA has built SD Express test fixtures that serve as adapters to existing PCI SIG Compliance Load Board as well as adapters for host testing. Those test fixtures are available by SDA or any of our approved test labs.

Figure 16 to Figure 18 show pictures of the available test fixtures. Card and host manufacturers may use them in the test labs or in their own facilities and utilize existing PCIe/ NVMe test equipment to perform compliance tests used by PCI SIG.

A similar set of test fixtures is available for SD 8.0 host and cards.
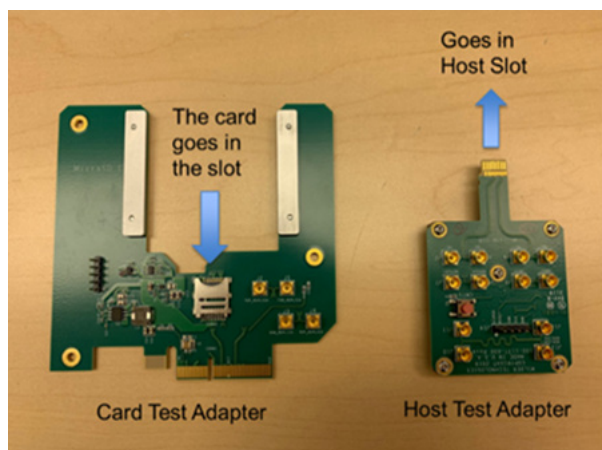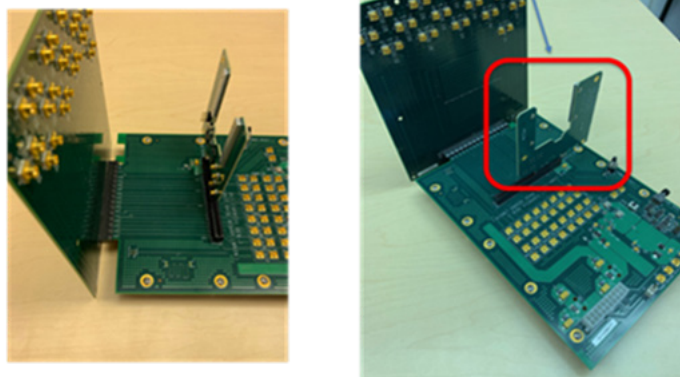

Figure 17 microSD Express Test Adapter Installed on Standard CBB as PCIe Add-in Card
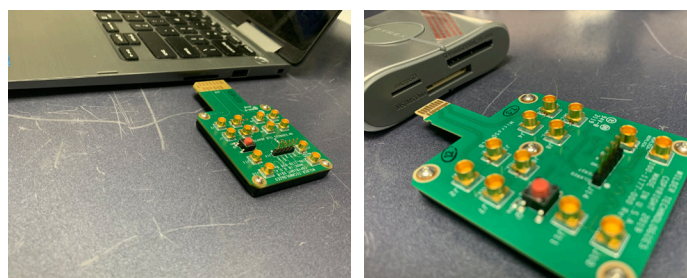
Figure 18 microSD Express and SD Express Host Test Adapters may be Inserted to Related SD Express Hosts

Figure 16 microSD Card and Host Test Adapters

Appendix A: Common Thermal Conducting Solutions

In addition to the thermal throttling mentioned in Section 6.2 of this document, or in Section 8.4.5 of the NVMe specification, thermal management and control also require a proper mechanical system design considering the thermal issues. There are various methods used today in the industry. Some of the commonly used methods are provided in this Appendix.

A.1 Host PCB/s Design

Proper thermal isolation from other heat dissipating elements and more PCB area around socket, in general, helps in heat spreading.

A.2 Heat Pipe

Hosts may use heat pipes for their processors. Research shows use of exclusive heat pipe helps to reduce card temperatures considerably.
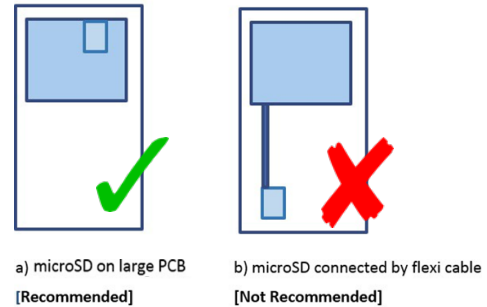

a) microSD on large PCB [Recommended]

b) microSD connected by flexi cable [Not Recommended]

Figure 19 Recommended PCB High-Level Design Concepts

Heat pipe thermal cycle
1) Working fluid evaporates to vapour absorbing thermal energy.
2) Vapour migrates along cavity to lower temperature end.
3) Vapour condenses back to fluid and is absorbed by the wick, releasing thermal energy
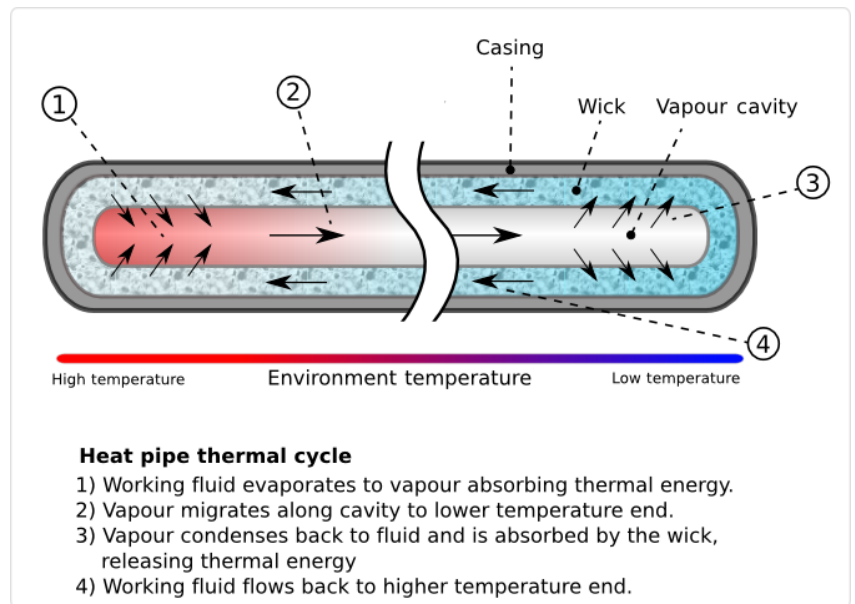4) Working fluid flows back to higher temperature end.

Figure 20 Heat Pipe

Source: https://commons.wikimedia.org/wiki/File:Heat_Pipe_Mechanism.png

Note: Careful routing of heat pipes required to disperse the heat away from hotspot to the colder regions in the system.

A.3 Graphene Tape

Heat spreader tapes are used often in all electronic devices to lower the hotspot temperature. In similar lines, it is recommended to use graphene tape which showed a temperature drop of a few degrees as per related research. Thicknesses ranging from 20-50 um are available in the market. Two methods of using graphene tape may be considered. First, it may be applied on the card itself. Second, the more beneficial method is to apply the tape to the connector and PCB, covering as large an area as possible. It can be used as a layer above card connector to uniformly distribute heat.
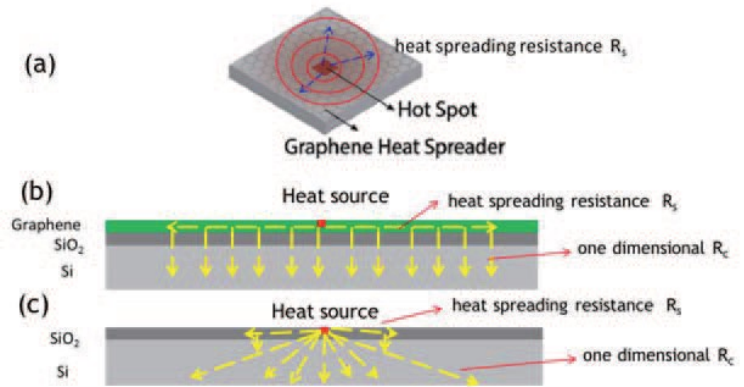

Figure 21 Graphene Tape

Reference: https://www.researchgate.net/publication/271551161_Characterization_for_graphene_as_heat_spreader_using_thermal_imaging_method

A.4 Connector Design

Minimizing thermal resistance between card/connector and between connector/host is critical. Changing connector material from stainless steel to brass or copper and having better thermal contact between connector and PCB to reduce air cavities helps to reduce card temperature.

A.5 Heat Sink and Fan Assembly

The proven heat sink and fan assembly is a go-to-option in cases where there are no space constraints. It is recommended to use blower type fan to get focused jet of air over the heat sink.

Appendix B:
Thermal Solutions for Gaming Products

Several examples for thermal solutions appropriate for use in gaming products and notebooks are provided in this appendix. All the solutions were provided by the Material and Chemical Research Laboratories at **Industrial Technology Research Institute (ITRI)**, Taiwan. Any questions and further requests of support may be provided by ITRI using the following points of contact:

Dr. Jeffrey Chiou (jeffreychiou@itri.org.tw) or Ms. Vicky Chen (vickychen@itri.org.tw).

The given material includes various terms as follows:

- MMC - Metal Matrix Composites
- CMC - Ceramic Matrix Composites
- TIM - Thermal Interface Materials
- CTE - Coefficient of Temperature Expansion
- OCC - Ohno Continuous Casting Process
- MCL - Materials and Chemical Laboratory
- UTS - Ultimate Tensile Strength
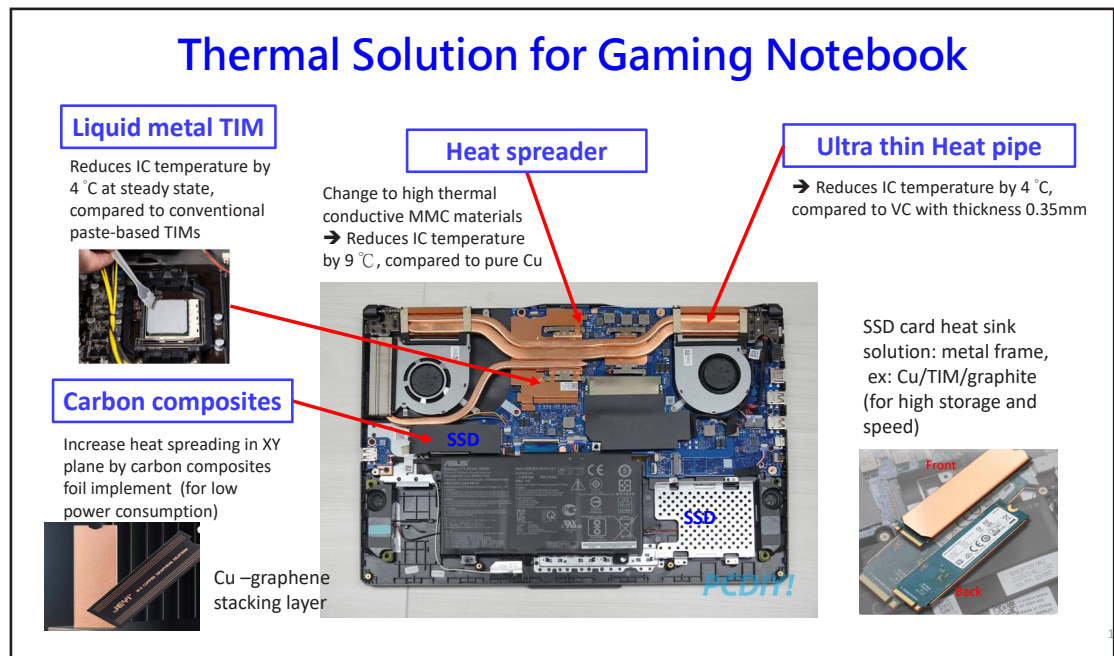- TDP - Thermal Design Power
- Cu - Copper

Thermal Solution for Gaming Notebook

Liquid metal TIM
Reduces IC temperature by 4 °C at steady state, compared to conventional paste-based TIMs

Heat spreader
Change to high thermal conductive MMC materials ➔ Reduces IC temperature by 9 ℃, compared to pure Cu

Ultra thin Heat pipe
➔ Reduces IC temperature by 4 ℃, compared to VC with thickness 0.35mm

SSD card heat sink solution: metal frame, ex: Cu/TIM/graphite (for high storage and speed)

Carbon composites
Increase heat spreading in XY plane by carbon composites foil implement (for low power consumption)

Cu –graphene stacking layer

SSD

SSD

Front

Back

Figure 22 Thermal Solutions for Gaming Notebook

Appendix B (cont'd): Thermal Solutions for Gaming Products

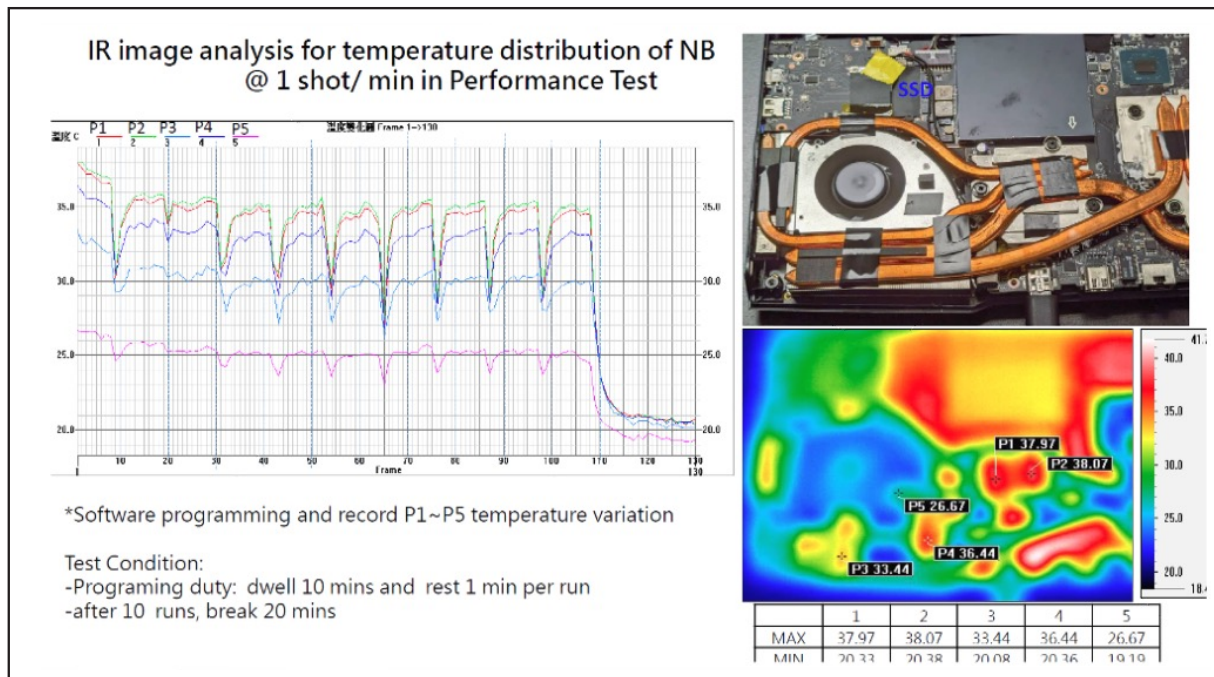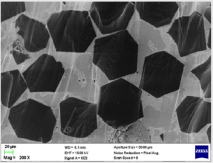*Figure 23 Image Analysis of Performance Test*

Heat Spreader for AI (GPU CPU) chip

	Al composites (CMC/MMC)	Cu composites (CMC/MMC)
Device structure		
Core technology	• High ceramic filling ratio • Heterogeneous bonding • Ultra High strength and light weight • No thermal crack treatment	• High ceramic filling ratio • Low temperature bonding technology • Fully dense with no voids • Forming and integrating with cooling modules
Device thickness (mm)	0.5~4.5 (adjective by customer design)	0.5~4.5 (adjective by customer design)
CTE (ppm/K)	8	6
Thermal conductivity (W/m·K)	606	715

Figure 24 Heat Spreader for AI

Appendix B (cont'd): Thermal Solutions for Gaming Products

Heat Pipe/Vapor Chamber

	Heat pipe	Vapor chamber
Device structure		
Core technology	• OCC continuous casting process • High Strength and high thermal conductivity Shell	• High Strength and high thermal conductivity Shell • Low Temperature Bonding Technology
Device thickness (mm)	1.5	0.3
Thermal resistance (°C/W)	0.3	0.14
Effective thermal conductivity (W/m·K)	> 4000	>5000

Figure 25 Heat Pipe/Vapor Chamber

Ultra-thin Highly Conductive Flexible Graphite Material
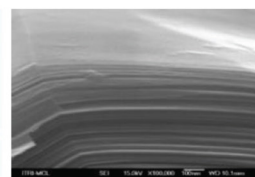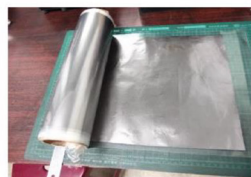
Thickness <20 um，thermal conductivity K~1600 W/m*k at XY direction   Laminate structure

	K (W/mK)	Graphited ratio (%)	Thickness (um)	Specialization properties
MCL	>1600 (XY plane)	93.5	<20um	Cu plated complex film

Flexible graphite with Cu plated

Figure 26 Ultra-thin Highly Conductive Flexible Graphite Materials

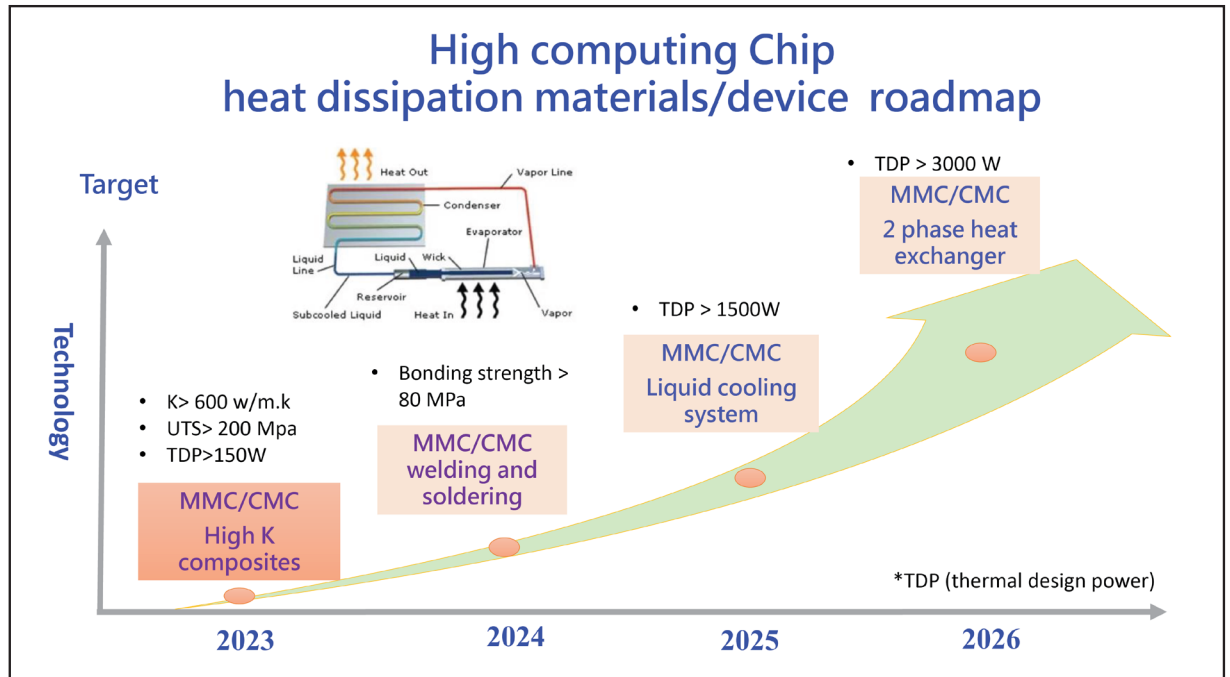## Appendix B (cont'd): Thermal Solutions for Gaming Products

Figure 27 High Computing Chip Heat Dissipation Materials and Device Roadmap

Appendix C:
Off-The-Shelf SD Express Host Solution

There may be existing off-the-shelf SD Express host solutions in the market that product manufacturers may choose to adopt.

BayHub Technology, Realtek, Genesys Logic and JMicron provide bridge solutions for SD Express support in host products and readers implementation as described in the following video and webinar slides.

Other off-the-shelf solutions may be available in the future[3].

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(3) The listed resources are companies known to the author at the publication date. Any other SDA members that supply such solutions are welcome to contact SDA office to be added in the provided list.